EE292K Project Description

This project is based on the paper(1) cited in reference and explores further ideas for power estimation of network processors to aid the development of scheduling algorithm based on reinforcement learning.

Motivation

With the increase in network traffic, the network processors operate at high speed to meet the high throughput rates. This fact, along with the increasing circuit densities make power a significant factor in the operation of the network processors or packet switches. The more the load, the more is the power consumption of the network system components. The load on the system can be used to determine if the system components can be slowed down or turned off, thereby compromising delay by a small amount for power. This necessiates power and delay aware scheduling algorithms for input queued packet switches.

The power and delay aware scheduling algorithm developed in (1) selects service vector that best aligns with the pending switch backlog and then scales the switch performance to optimize the average power delay tradeoff for the switch. This two step algorithm sequence is repeated for every packet transfer period.

Problem description

As explained in (1),the scheduling algorithm aims to minimize the two terms- power consumption and packet delay.The power consumption of the packet switch is $P = (1/2)\alpha CV^2 f$, C is the capacitance driven by the device, V is the voltage supply, f is the device clock frequency, α is the activity factor of the device.

Power consumption of a switch can be adjusted by varying the clock frequency of the device, varying its voltage supply and powering up or down the portions of the switch as necessary. Changing the supply causes a quadratic cost in power, while changing frequency or powering up/down causes linear cost. In general, if the cost is $F(s^t)$ as a function of service vector s^t , the power cost is the summation of $(s^t)F(s^t)$ over period of time.

Packet delay is measured by the backlog cost. A packet arriving in a longer queue will have a shorter delay than the packet arriving in a shorter queue. If the backlog vector is x^t , then the backlog cost is the summation of $(x^t)F(x^t)$ over period of time.

Hence scheduling algorithm intends to minimize the following function,
$J(x^t) = \Sigma \ ((s^t)F(s^t) + (x^t)F(x^t))$

In this work, the focus is on the estimation of the power cost function $F(s^t)$ for the switch. A novel idea or methodology is to be developed to estimate the power cost for various components or blocks in the network processor, taking into account the architecture of a typical network processor.

Reference

(1) Lykomidis Mastroleon, Daniel O' Neill, Benjamin Yolken and Nicholas Bambos ,“Power and Delay Aware Management of Packet Switches” , IEEE Transactions on Computers, October 2011.
(2) http://www.barrgroup.com/Embedded-Systems/How-To/Network-Processors